

Notice of References Cited	Application/Control No. 10/721,260	Applicant(s)/Patent Under Reexamination SAKATA, TOYOKAZU	
	Examiner Patricia A. George	Art Unit 1765	Page 1 of 1

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	M	US-			

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NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	Lin et al.; An Optimized Integration Scheme for 0.13 um Technology Node Dual-Damascene Cu Interconnect; 0-7803-6327—2/00 © 2000 IEEE
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*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
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